Cellron

Datasheet

Version 1.1

Teleron

About This Document

This document provides the specifications for the Cellron development board module.

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1. Overview

Cellron is a powerful general Wi-Fi+BT+LTE MCU module targeting a wide range of applications, from low-power sensor networks to the most demanding tasks such as audio encoding, music streaming and MP3 decoding.

At the center of this module is the ESP32-Wroom chip. The embedded chip is designed to be scalable and adaptable. There are two CPU cores that can be controlled separately, and the CPU clock frequency is adjustable from 80 MHz to 240 MHz. The user can also turn off the CPU and The chip also has a low-power coprocessor that can be used instead of the CPU to save power while performing tasks that do not require much computing power, such as monitoring of peripherals. ESP32 integrates a rich set of peripherals such as capacitive touch sensors, Hall sensors, SD card interface, Ethernet, high speed SPI, UART, I2S and I2C.

The integration of Bluetooth, Bluetooth LE, Wi-Fi and 4G-LTE ensures that a wide range of applications can be targeted, and that the module is all-around: using Wi-Fi allows a large physical range and direct connection to the Internet through a Wi-Fi or 4G-LTE module. Wi-Fi or 4G-LTE module, while using Bluetooth, allows the user to conveniently connect to the phone or broadcast low energy beacons for detection. The sleep current of the ESP32 chip is less than 5 μA, making it suitable for battery-powered and wearable electronics applications. The module supports up to 150 Mbps data rate and 20 dBm output power at antenna to provide the widest physical range. Therefore, the module offers industry-leading features and the best performance for electronic integration, range, power consumption and connectivity.

Table 1 provides the specifications of Cellron .

Table 1: Cellron Specifications

Categories	Items	Specifications
Wi-Fi	Protocols	802.11 b/g/n (802.11n up to 150 Mbps)
		A-MPDU and A-MSDU aggregation and 0.4 μs guard interval support
	Frequency range	2.4 GHz ~2.5 GHz
Bluetooth	Protocols	Bluetooth v4.2 BR/EDR and Bluetooth LE specification
	Radio	NZIF receiver with –97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
Hardware	Module interfaces	SD card, UART, SPI, SDIO, I2C, LED PWM, Motor PWM, I2S, IR, pulse counter, GPIO, capacitive touch sensor, ADC, DAC
	On-chip Sensor	Hall sensor
	Integrated crystal	40 MHz crystal
	Integrated SPI flash	4 MB
	Operating voltage/ Power supply	2.7 V ~ 3.6 V
	Operating current	Average: 80 mA
	Minimum current delivered by power supply	500 mA
	Recommended Operating Temperature Range	–40 °C ~+85 °C
	Package size	(18.00±0.10) mm × (25.50±0.10) mm × (3.10±0.10) mm

2. Pin Definitions

2.1 Pin Layout

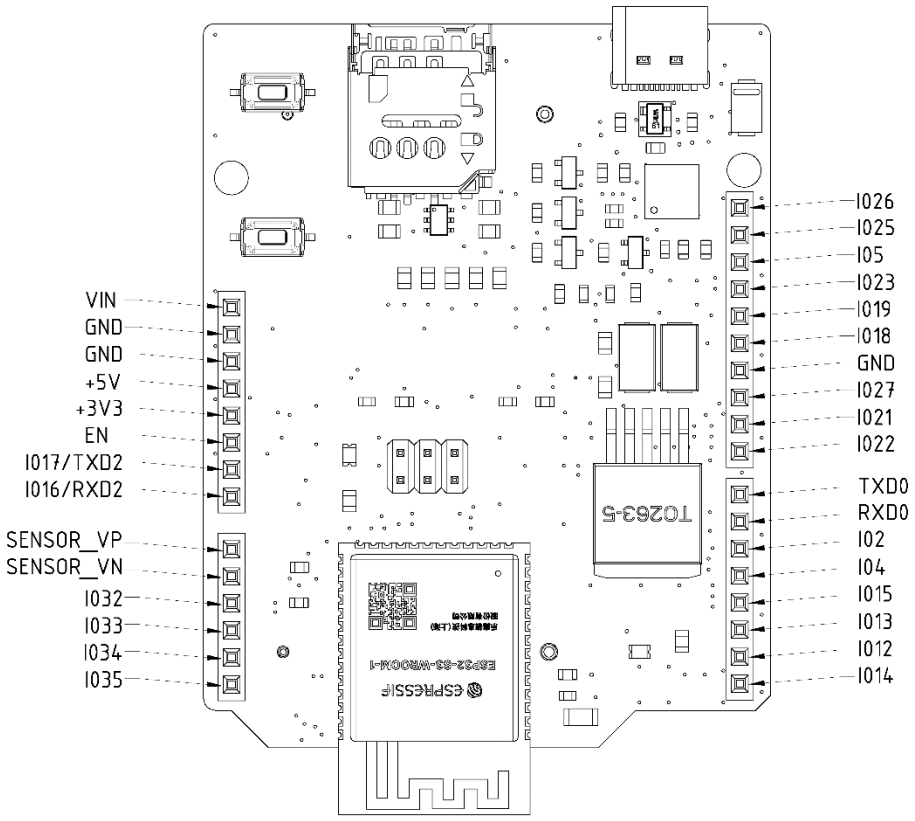

Figure 1: Cellron Pin Layout (Top View)

2.2 Pin Description

Cellron has 38 pins. See pin definitions in Table 2.

Table 2: Pin Definitions

Name	No.	Type	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	**I**	Module-enable signal. Active high.
SENSOR_VP	4	**I**	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_VN	5	**I**	GPIO39, ADC1_CH3, RTC_GPIO3
IO34	6	**I**	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	7	**I**	GPIO35, ADC1_CH7, RTC_GPIO5
IO32	8	**I/O**	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	9	**I/O**	GPIO33,XTAL_32K_N(32.768kHzcrystaloscillatoroutput),ADC1_CH5, TOUCH8, RTC_GPIO8

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IO25	10	**I/O**	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	11	**I/O**	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	12	**I/O**	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	13	**I/O**	GPIO14,ADC2_CH6,TOUCH6,RTC_GPIO16,MTMS,HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	14	**I/O**	GPIO12,ADC2_CH5,TOUCH5,RTC_GPIO15,MTDI,HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
GND	15	P	Ground
IO13	16	**I/O**	GPIO13,ADC2_CH4,TOUCH4,RTC_GPIO14,MTCK,HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
SHD/SD2*	17	**I/O**	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
SWP/SD3*	18	**I/O**	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
SCS/CMD*	19	**I/O**	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS
SCK/CLK*	20	**I/O**	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
SDO/SD0*	21	**I/O**	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
SDI/SD1*	22	**I/O**	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
IO15	23	**I/O**	GPIO15,ADC2_CH3,TOUCH3,MTDO,HSPICS0,RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	24	**I/O**	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	25	**I/O**	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	26	**I/O**	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
IO16	27	**I/O**	GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT
IO17	28	**I/O**	GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180
IO5	29	**I/O**	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	30	**I/O**	GPIO18, VSPICLK, HS1_DATA7
IO19	31	**I/O**	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
NC	32	**-**	-
IO21	33	**I/O**	GPIO21, VSPIHD, EMAC_TX_EN
RXD0	34	**I/O**	GPIO3, U0RXD, CLK_OUT2
TXD0	35	**I/O**	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO22	36	**I/O**	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
IO23	37	**I/O**	GPIO23, VSPID, HS1_STROBE
GND	38	P	Ground

NOTE:

- Pins SCK/CLK, SDO/SD0, SDI/SD1, SHD/SD2, SWP/SD3 and SCS/CMD, namely GPIO6 to GPIO11, are connected to the integrated SPI flash integrated on the module and are not recommended for other uses.

3. Functional Description

This section describes the modules and functions integrated into the Cellron board.

3.1 CPU and Internal Memory

The Cellron board contains one low power esp32 wroom 32 microprocessor. Internal memory includes:

- 448 KB ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; Accessed by the main CPU during RTC Boot from Deep-sleep mode.
- The 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the coprocessor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system and the remaining 768 bits are reserved for customer applications, including flash encryption and chip ID.

3.2 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM via high speed caches.

- The external flash can be mapped into CPU instruction memory space and read-only memory space at the same time.
  - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
  - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped to the CPU data memory area. Up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

Cellron board integrates a 4MB SPI flash, which is connected to GPIO6, GPIO7, GPIO8, GPIO9, GPIO10 and GPIO11. These six pins cannot be used as regular GPIOs.

3.3 Crystal Oscillators

The module uses a 40 MHz crystal oscillator.

3.4 RTC and Low Power Management

With the use of advanced power management technologies, Cellron can switch between different power modes.

4. Peripherals and Sensors

NOTE:

- External connections can be made to any GPIO except GPIOs in the 6 to 11 range.
- These six GPIOs are connected to the module's integrated SPI flash.

5. Electrical Characteristics

5.1 Absolute Maximum Values

Voltages above the absolute maximum values listed in Table 3 below can cause permanent damage to the device.

Table 3: Absolute Maximum Values

Symbol	Parameter	Min	Max	Unit
VDD	Power supply voltage	–0.3	7.6	V
I_{output}[1]	Cumulative I/O output current	-	1,100	mA
T_{store}	Storage temperature	–40	150	°C

5.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	Power supply voltage	2.7	5.0	7.6	V
I_{VDD}	Current delivered by external power supply	0.5	-	-	A
T	Operating temperature	–40	-	85	°C

5.3 DC Characteristics (3.3 V, 25 °C)

Table 5: DC characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		-	2	-	pF
V_{IH}	High-level input voltage		0.75×VDD[1]	-	VDD[1]+0.3	V
V_{IL}	Low-level input voltage		–0.3	-	0.25×VDD[1]	V
I_{IH}	High-level input current		-	-	50	nA
I_{IL}	Low-level input current		-	-	50	nA
V_{OH}	High-level output voltage		0.8×VDD[1]	-	-	V
V_{OL}	Low-level output voltage		-	-	0.1×VDD[1]	V
I_{OH}	High-level source current	VDD3P3_CPUpowerdomain[1, 2]	-	40	-	mA
		VDD3P3_RTCpowerdomain[1, 2]	-	40	-	mA
		VDD_SDIO power domain [1, 3]	-	20	-	mA

Symbol	Parameter	Min	Typ	Max	Unit
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)	-	28	-	mA
R_{PU}	Resistance of internal pull-up resistor	-	45	-	kΩ
R_{PD}	Resistance of internal pull-down resistor	-	45	-	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip	-	-	0.6	V

Notes:

1. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, VOH >=2.64 V, as the number of current-source pins increases.

2. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

6. Physical Dimensions

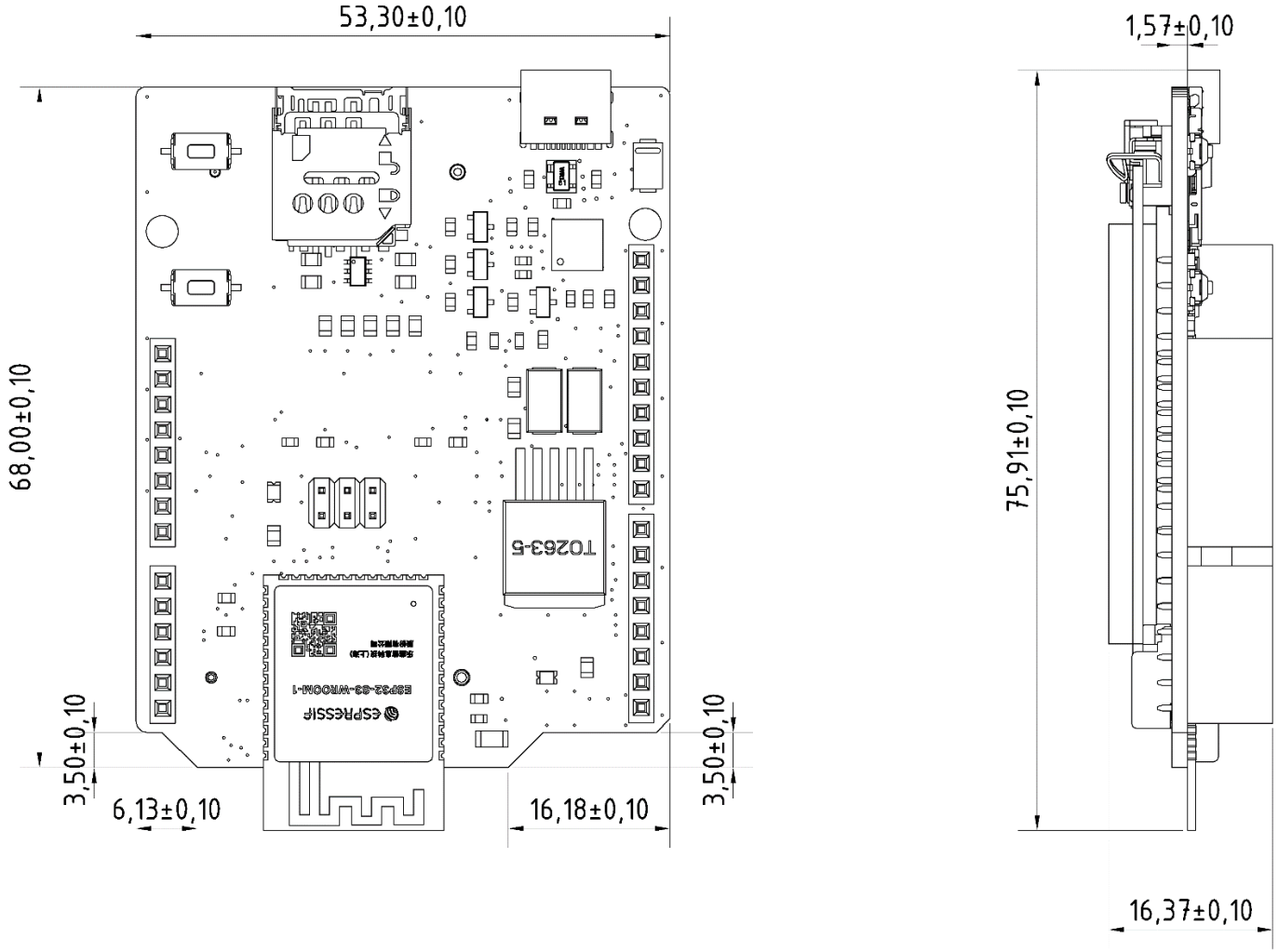

Figure 2: Physical Dimensions of Cellron